OCTAVE S/C-BAND MMIC T/R MODULES FOR MULTI-FUNCTION PHASED ARRAYS

J. J. Komiak
General Electric
Electronics Laboratory
Syracuse, New York

A. K. Agrawal
General Electric
Government Electronic Systems Department
Moorestown, New Jersey

Abstract

A complex wideband Transmit/Receive Module that has achieved performance levels superior to any MMIC module will be described. Performance across an octave 3.0 to 6.0 GHz band includes a power output of 21 Watts at S-Band and 19 at C-Band, a noise figure of 3.9 to 5.0 dB, 30 to 38 dB of receive gain, 25 to 26 dBm IP_3, 40 dB of gain control in 256 steps, dual receive channels with independent amplitude and phase control, and an 8-bit phase shifter with less than 1 degree calibrated RMS phase error. Total GaAs area is 146 mm^2 with 170 mm of total gate periphery. The module incorporates a compact digital interface, requires only three supply voltages, and utilizes advanced packaging techniques, resulting in a size compatible with a grating lobe free grid spacing.

Introduction

In order to maximize performance and minimize the cost of this module a shared leg architecture shown in Figure 1 was selected. The shared leg, used for both transmit and receive, includes a variable gain amplifier, phase shifter, and gain blocks. Connection to either the final output amplifiers on transmit or the LNA on receive is accomplished through the use of a DPDT transfer switch. Independent phase and amplitude control channels are implemented on receive. This implementation circumvents many of the difficulties in achieving phase and amplitude tracking between the three complex beamforming networks required of a monopulse radar [1].

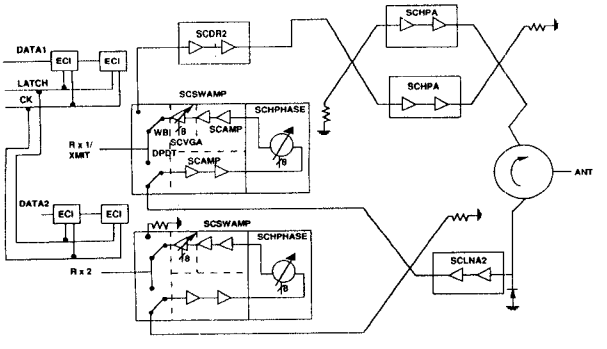


Figure 1: Block Diagram of S/C-Band T/R Module

MMIC Chip Set

The shared leg has been partitioned into an RF-testable two chip set, an 8-bit phase shifter (SCPHASE), and an integrated "super-chip" incorporating a DPDT transfer switch, an 8-bit variable gain amplifier, and four stages of gain blocks (SCSWAMP). These chips were fabricated at Harris Microwave Semiconductor using their 0.5 μm G10 implant process. The wafer-probeable phase shifter shown in Figure 2, is based on an extensive effort at GE in researching and optimizing phase shifter topology for not only RF performance, but process insensitivity and high yield. The 180, 90, and 45 degree bits are FET-switched high-pass/low-pass structures, the 22 and 11 degree bits are FET-switched bridged T's, while the three LSB's are resonated FET's. Chip size is 3.8 mm x 3.3 mm, while the typical performance across the 256 phase states is 10 dB insertion loss, ± 1.0 dB maximum amplitude variation with less than 1 degree calibrated RMS phase error.

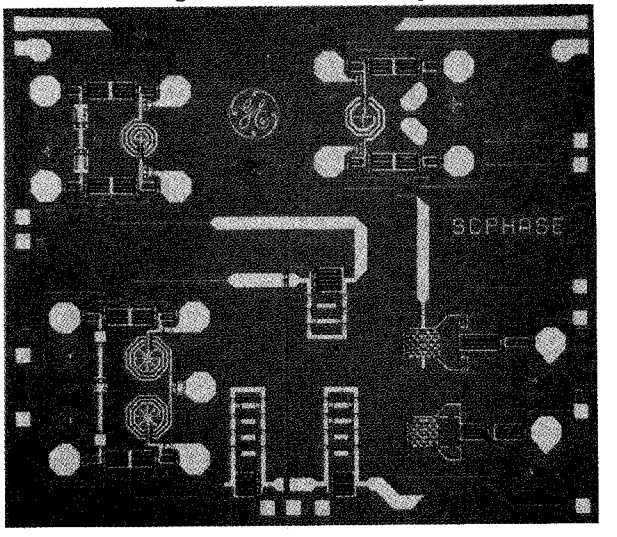


Figure 2: Phase Shifter MMIC (SCPHASE)

The SCSWAMP "super-chip" shown in Figure 3, is a wafer-probeable MMIC incorporating a transfer switch, gain blocks, and a variable gain amplifier. The DPDT transfer switch is a wideband DC-18 GHz design using series and shunt FET's as switching elements. The variable gain amplifier is based upon the segmented dual gate FET approach [2,3]. The gain blocks are based upon a self-biased shunt feedback amplifier for process insensitivity, and flat gain/good VSWR across the 3.0 to 6.0 GHz band. Chip size is 3.8 mm x 4.7

91CH3016-3/91/0000-0035$01.00 © 1991 IEEE

mm, while typical performance is 9 dB forward path and 19 dB reverse path gain, with over 40 dB of gain control range in 256 linear voltage steps. Third order intercept point ranges from +25 to +26 dBm across 3.0 to 6.0 GHz.

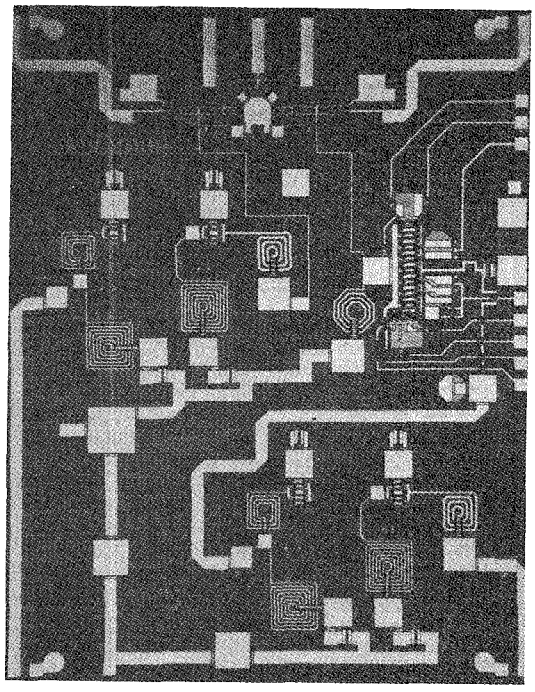


Figure 3: Switch/Amplifier MMIC (SCSWAMP)

The MMIC power amplifier (SCHPA) shown in Figure 4, has established a new standard for power output and bandwidth in MMIC form [4]. Chip size is 5.8 mm x 4.3 mm, while the output network measures 8.7 mm x 8.2 mm. Typical performance of the power amplifier versus frequency for a constant power input is a power output of 11 Watts + 1 dB with an associated power gain of 10.5 to 12.5 dB. Small-signal gain is 16 to 24 dB and power-added efficiency ranges from 10 % to 17 %.

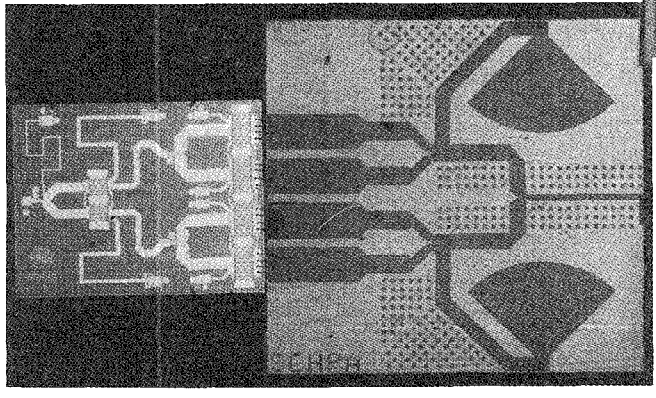


Figure 4: Power Amplifier MMIC (SCHPA)

The driver amplifier (SCDR2) shown in Figure 5, like the power amplifier was processed at Harris Microwave Semiconductor using their 0.5 µm P5 implant process. It produces 2 to 4 Watts with 16 dB power gain at 10 % to 18 % power-added efficiency from 3.0 to 6.0 GHz. Chip size is 4.6 mm x 4.2 mm while the output network measures 4.0 mm x 3.0 mm.

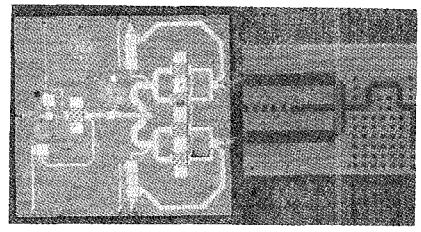


Figure 5: Driver Amplifier MMIC (SCDR2)

The two-stage MMIC low noise amplifier (SCLNA2) shown in Figure 6, is based upon a 0.5 µm x 600 µm eight finger interdigitated HEMT device fabricated on selectively doped AlGaAs/GaAs heterostructures grown by molecular beam epitaxy (MBE). The amplifier was fabricated at the General Electric Electronics Laboratory using a hybrid process consisting of optical stepper projection lithography with E-beam defined gates. Chip size measures 3.9 mm x 1.6 mm. Typical performance versus frequency is 16 to 18 dB of gain from 3.0 to 6.0 GHz with a noise figure of less than 2.4 dB, averaging 1.8 dB. Third-order intercept point of the MMIC amplifier ranges from +25 dBm to +27 dBm.

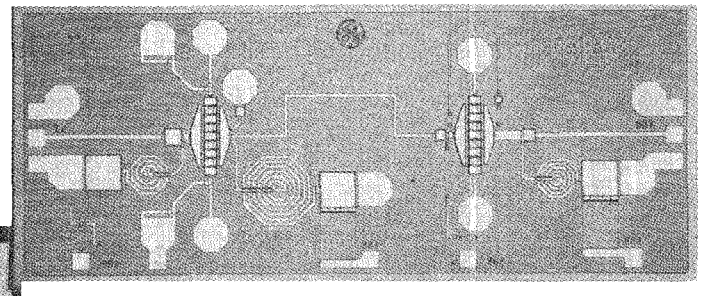


Figure 6: Low Noise Amplifier MMIC (SCLNA2)

The Element Control Interface Chip (ECI) shown in Figure 7, functions as a serial-in/parallel-out shift-register/latch/driver, accepting serial TTL digital data input, providing appropriate voltage level outputs, and synchronized timing for T/R module mode switching. The ECI, implemented in Tri-Quint Enhancement/Depletion digital GaAs using low power Buffered FET Logic provides these functions with output levels appropriate for the Harris 0.5 µm G-10 process. The ECI is capable of switching and settling the worst case capacitive load of the VGA at 15 pF in less than 100 nsec. Clock rate is 25 MHz, while chip size is 2.3 mm x 1.0 mm.

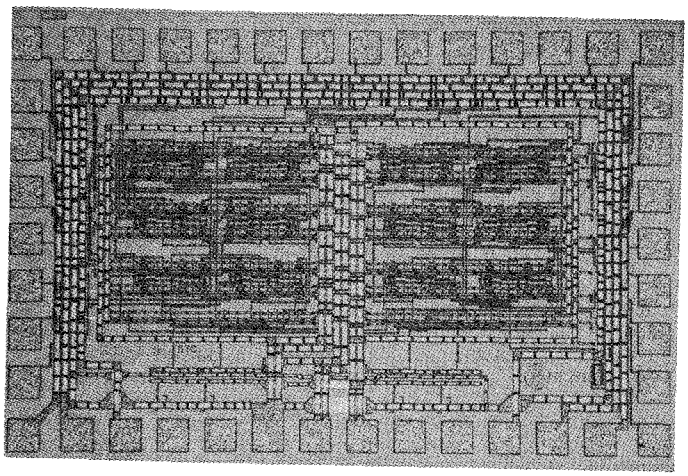


Figure 7: Element Control Interface Chip (ECI)

Module Construction

Figure 8 is a photograph of the wideband S/C-Band T/R Module. The package is a low parasitic, hermetic structure composed of base, ceramic mother substrate, ceramic wall, and lid. The mother substrate incorporates all RF circuitry on the top surface with thin film TaN resistors for voltage conditioning/50 Ω terminations and thick film multi-layer DC and control distribution on the backside. A full thick film plane has been devoted to HPA voltage distribution. Backside thick film ground planes minimize coupling and provide the reference ground plane for the frontside microstrip circuitry. Module size including the external circulator and lid is 4.4" x 1.16" x 0.5 ", which is compatible with the grid spacing required for grating lobe free operation.

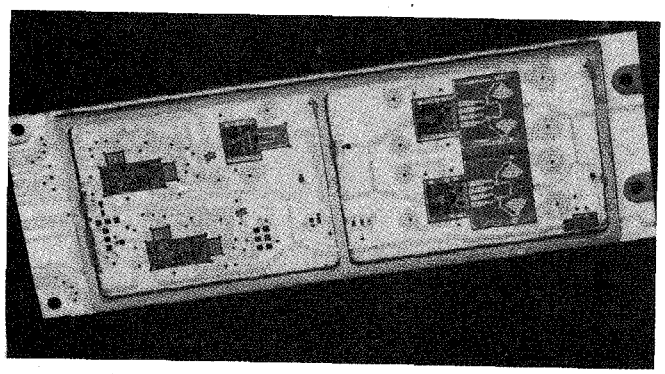


Figure 8: Wideband S/C-Band T/R Module

Measured Performance

Figure 9 shows the receive gain of the module from 3.0 to 6.0 GHz for all 256 VGA states. Across a 30 dB adjustment range, the incidental phase shift is less than 8.9 degrees RMS, and below 3 degrees RMS across 90 % of the 3.0 to 6.0 GHz band. Figure 10 is the response for all 256 phase states. Calibrated RMS phase error is less than 1 degree with less than 1.2 dB RMS amplitude variation. The worst case match at the beamformer port was 2.3:1, while at the antenna port, worst case was 3:1. Over 70% of the band, both ports are better than 1.5:1. Noise figure response, shown in Figure 11, is 3.9 dB at S-Band, slowly rising to 5 dB at C-Band. IMD products, shown in Figure 12, are -55 dBc for a -35 dBm input at each tone, resulting in a +25 to +26 dBm third order intercept point. Power output, shown in Figure 13, is 21 Watts at S-Band and 19 Watts at C-Band. The module requires 5.5 V at 600 mA and -3.5 V at 160 mA in receive and an additional 9 V at 16 A during transmit.

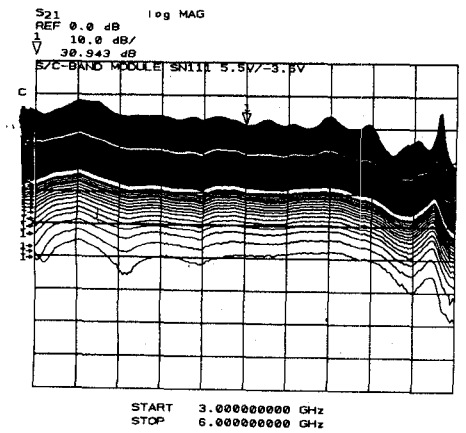


Figure 9: Receive Gain of S/C-Band T/R Module (256 VGA States)

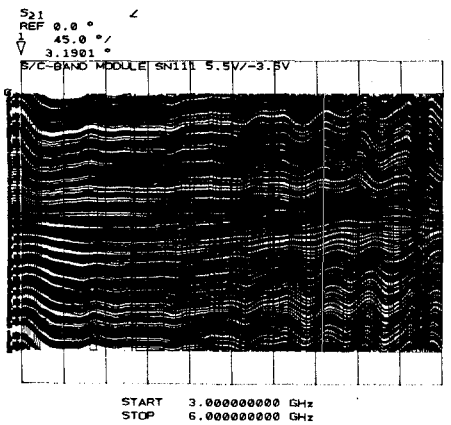


Figure 10: Phase Shift of S/C-Band T/R Module (256 Phase States)

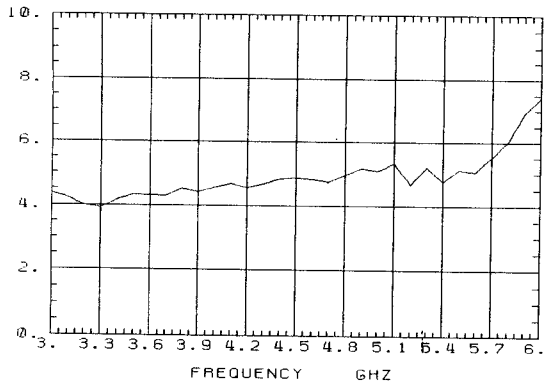


Figure 11: Noise Figure Response of S/C-Band T/R Module

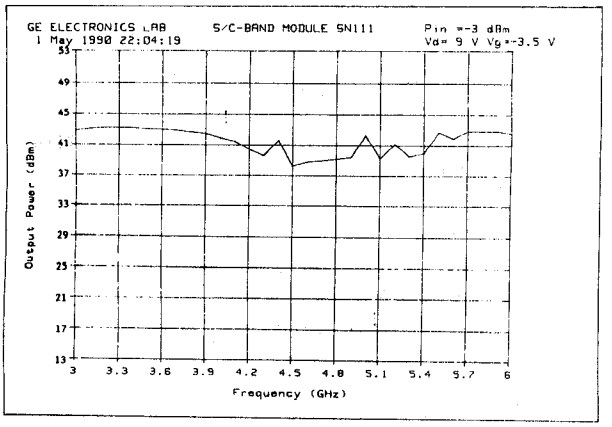
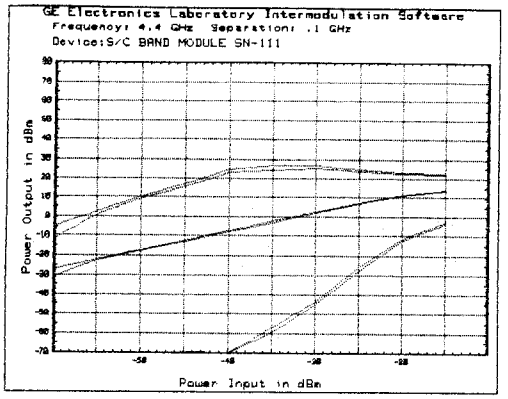


Figure 13: Power Output of S/C-Band T/R Module (Pulse Width = 100 μsec, Duty Cycle = 5 %)



In. Power (dBm/Tone)	IMD 1 (dBm)	Tone 1 (dBm)	Tone 2 (dBm)	IMD 2 (dBm)	Gain1 (dB)	Gain2 (dB)	Intercept Points (dBm) Min	Max
-10.00	3.10	15.30	14.70	1.80	25.30	24.70	20.50	22.05
-15.00	-2.60	13.90	13.70	-3.40	28.90	28.70	21.85	22.55
-20.00	-11.20	11.40	11.30	-12.50	31.40	31.30	22.55	23.35
-25.00	-25.75	7.30	7.10	-27.65	32.30	32.10	23.52	24.77
-30.00	-43.65	2.60	2.10	-45.25	32.60	32.10	24.98	26.52
-35.00	-57.10	-2.20	-2.90	-59.90	32.80	32.10	24.20	26.65
-40.00	-70.40	-7.20	-7.90	-69.90	32.80	32.10	23.10	24.40
-45.00	-70.90	-12.20	-12.90	-69.40	32.80	32.10	15.35	17.15
-50.00	-71.50	-17.30	-17.60	-72.00	32.70	32.40	9.35	10.05
-55.00	-69.80	-22.15	-22.45	-71.40	32.85	32.55	1.23	2.48
-60.00	-69.90	-27.35	-31.05	-71.70	32.65	28.95	-11.63	-5.18

Noise Level (approx.)= -74.9 dBm

Figure 12: IMD Response of S/C-Band T/R Module

Acknowledgment

The authors would like to acknowledge the many individuals at General Electric who contributed to the design, fabrication, and processing of the described circuits. In particular, A. Jacomb-Hood, C. Grondahl, and T. Cokinos for MMIC design, E. Lewis for MMIC layout, W. Kong for HEMT processing, C. Low, A. Sun, and M. Katz for module fabrication, A. Thatcher for assembly, R. Clark and S. Miller for module engineering, and H. Marcus for mechanical design. We would also like to acknowledge the contributions of Harris Microwave Semiconductor and Tri-Quint Semiconductor for foundry service.

References

[1] A. K. Agrawal, N. R. Landry, "Independent Control of Sum and Difference Patterns in Active Phased Array Antennas," 1989 IEEE International Antennas and Propagation Symposium Digest, San Jose, CA, June 26-30, 1989, pp 392-395.

[2] K. H. Snow, J. J. Komiak, D. A. Bates, "Segmented Dual-Gate MESFET's for Variable Gain and Power Amplifiers in GaAs MMIC," IEEE Transactions, Vol. MTT-36, No. 12, December 1988, pp 1976-1985.

[3] U. S. Patent 4638190, 4734751, 4901032, and others pending.

[4] J. J. Komiak, "Design and Performance of an Octave Band 11 Watt Power Amplifier MMIC," IEEE Transactions, Vol. MTT-38, No. 12, December 1990, pp 2001-2006.